In the Claims:

**Please amend claims 1, 6, 7, 11, 12, 13, 15, 17, 19, and 21 and cancel claims 4 and 10 such that the claims read as follows:**

1. (Currently amended) A method for testing an integrated circuit (IC) comprising:

selecting a bit <u>during an ABIST test</u> from each of a plurality of memory arrays formed on an IC chip;

selecting one of the plurality of memory arrays; and

storing the selected bit from the selected memory array.

2. (Original) The method of claim 1 wherein selecting a bit from each of a plurality of memory arrays includes selecting a wordline in each of the plurality of memory arrays.

3. (Original) The method of claim 1 wherein selecting a bit from each of a plurality of memory arrays includes overwriting an initial state bit value of a selection circuit with a value of the selected bit.

4. (Original) The method of claim 1 wherein storing the selected bit from the selected memory array includes storing the selected bit from the selected memory array in a latch.

5. (Original) The method of claim 1 wherein storing the selected bit from the selected memory array includes one of storing an initial state bit value of an output of a selection circuit and storing a modified initial state bit value of the output of the selection circuit in the latch.

6. (Currently amended) The method of claim 1 wherein ~~selecting a bit from each of a plurality of memory arrays formed on an~~

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~~integrated circuit chip,~~ selecting one of the plurality of
memory arrays, and storing the selected bit from the selected
memory array are performed during an ABIST test of the
integrated circuit chip.

7.    (Currently amended) A method for testing an integrated
circuit (IC) comprising:
    selecting a bit during an ABIST test from each of a first
and second plurality of memory arrays formed on an IC chip;
    selecting one memory array from each of the first and
second plurality of memory arrays; and
    storing the selected bit from the selected memory array for
each of the first and second plurality of memory arrays.

8.    (Original) The method of claim 7 wherein selecting a bit
from each of the first and second plurality of memory arrays
includes selecting a wordline in each of the first and second
plurality of memory arrays.

9.    (Original) The method of claim 7 wherein selecting a bit
from each of the first and second plurality of memory arrays
includes:
    overwriting the first initial state bit value with a value
of the selected bit from the selected memory array of the first
plurality of memory arrays; and
    overwriting a second initial state bit value with a value
of the selected bit from the selected memory array of the second
plurality of memory arrays.

10.    (Original) The method of claim 7 wherein storing the
selected bit from the selected memory array for each of the
first and second plurality of memory arrays includes:

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storing the selected bit from the selected memory array of the first plurality of memory arrays in a first latch; and

storing the selected bit from the selected memory array of the second plurality of memory arrays in a second latch.

11.  (Original) The method of claim 10 wherein storing the selected bit from the selected memory array of the first plurality of memory arrays includes one of storing an initial state bit value of an output of a first selection circuit and storing a modified initial state value of the output of the first selection circuit in a first latch; and

    wherein storing the selected bit from the selected memory array of the second plurality of memory arrays includes one of storing an initial state bit value of an output of a second selection circuit and storing a modified initial state value of the output of the second selection circuit in a second latch.

12.  (Currently amended) The method of claim 7 wherein ~~selecting a bit from each of a first and second plurality of memory arrays formed on an IC chip,~~ selecting one memory array from each of the first and second plurality of memory arrays, and storing the selected bit from the selected memory array for each of the first and second plurality of memory arrays are performed during an ABIST test of the IC chip.

13.  (Currently amended) An apparatus comprising:

    a plurality of memory arrays;

    a latch;

    a selection circuit coupled to the plurality of memory arrays and to the latch, and ~~adapted~~ operative to:

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receive a bit _during an ABIST test_ from each of the
plurality of memory arrays;

select one of the plurality of memory arrays; and

store the bit from the selected memory array.

14.  (Original) The apparatus of claim 13 further comprising a
decoder coupled to the selection circuit.

15.  (Currently amended) The apparatus of claim 14 wherein the
decoder is ~~adapted~~ _operative_ to generate signals used to select
one of the plurality of memory arrays.

16.  (Original) The apparatus of claim 13 wherein the selection
circuit comprises a multiplexer.

17.  (Currently amended) An apparatus comprising:

a first plurality of memory arrays;

a first latch;

a first selection circuit coupled to the first plurality of
memory arrays and to the first latch, and ~~adapted~~ _operative_ to:

(a)  receive a bit _during an ABIST test_ from each of the
first plurality of memory arrays;

(b)  select one of the first plurality of memory arrays;
and

(c)  store the bit from the selected one of the first
plurality of memory arrays;

a second plurality of memory arrays;

a second latch;

a second selection circuit coupled to the second plurality
of memory arrays and to the second latch, and _operative_ ~~adapted~~
to:

(d)  receive a bit during an ABIST test from each of the second plurality of memory arrays;

(e)  select one of the second plurality of memory arrays; and

(f)  store the bit from the selected one of the second plurality of memory arrays.

18.  (Original) The apparatus of claim 17 further comprising a decoder coupled to the first and second selection circuits.

19.  (Currently amended) The apparatus of claim 18 wherein the decoder is ~~adapted~~ operative to generate signals used to select one memory array from each of the first and second plurality of memory arrays.

20.  (Original) The apparatus of claim 17 wherein the first and second selection circuit comprise multiplexers.

21.  (Currently amended) The apparatus of claim 17 wherein the first and second selection circuits are ~~adapted~~ operative to perform (a)-(c) and (d)-(f) simultaneously.